"Intelligent Control Design of PMSM Drive for Automotive Applications"

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Abstract - This paper describes the practical design considerations of Permanent Magnet Synchronous Motor (PMSM) drive for Electric Power Steering (EPS) Used in Automotive application. The design of various Blocks of PMSM Drive is discussed in detail. The experimental results show that the control & power circuit used in the design can achieve excellent and consistent torque & speed performance and is well suited for EPS application.

Keywords— Electric power Steering, Permanent magnet synchronous machine. Permanent magnet material, MOEFET Inverter circuit, clock signal generator, address generator, EPROM.

I. Introduction

PERMANENT-MAGNET synchronous motor (PMSM) drives are, due to their high efficiency and power density, attractive for a variety of applications [1], [2]. In vehicles, electric drives can replace traditional mechanical actuators to achieve advantages such as higher efficiency and improved dynamical performance. Electric Power Steering(EPS) systems have attracted much attention for their advantages with respect to improved fuel consumption(saving 3~6%, reduction of weight 3~5kg) and have been widely adopted as automotive power steering equipment in recent years. The permanent magnetic field Direct Current (DC) motors are widely used for EPS system, but nowadays many engineers are trying to adopt the Permanent Magnet Synchronous motor(PMSM). It is because the fact that motor vibration and torque fluctuations are directly transferred through the steering wheel to the hands of the driver must be considered For automotive applications, reliability and cost are major concerns. Generally, power electronic converter topologies with reduced component counts can reduce the size, weight, and cost of the converter and can also improve reliability [3].

Permanent magnet synchronous motor is used here with three stator windings for the motor operation. Three supply voltages are obtained with the help of three phase MOSFET bridge inverters. MOSFET bridges are fed with fixed dc voltage which is obtained by rectifying ac voltage available from ac mains with the help of Diode Bridge. Shunt capacitor filter is used for filtering purpose. Operation of the MOSFET Bridge is controlled by the control circuit. Gating pulses required to turn the MOSFET ON are obtained from the control circuit. By controlling the frequency of the gating pulses frequency of the output from MOSFET bridge is controlled. Control circuit consists of clock generator counter and EPROM. First data required to generate gating pulses is calculated and is stored in EPROM. This data is outputted at the output of the EPROM by generating the address of the memory location with the help of 4 bit binary ripple counter. Clock input required for the operation of the counter is generated using IC 555 in astable mode. Frequency of the gating signals coming out of EPROM is dependent on the frequency with which addressing is done which is turn dependent on the clock frequency. Thus by varying the clock frequency of gating signal is varied. If frequency of gating signal is varied, then the MOSFET bridge output frequency is also varied. Thus we obtain variable frequency output. Gating signal outputted by EPROM cannot be directly applied to MOSFET bridge as they are very weak. So isolator and driver circuit is used. Necessary isolation of low power control circuit from high power bridge circuit is obtained by using opt isolator. In interior or buried magnet synchronous motor (IPM), the magnets are mounted inside the rotor. The motor is connected on load and its speed depends on the stator supply frequency.

This paper presents some practical design considerations and trade-offs for the PMSM drive system for EPS application. Section 2 describes design considerations. Section 3 presents some experimental results. Section 4 is the conclusion...

II. PMSM Drive Design Considerations

The following aspects of the system design are described in this section: PMSM drive architecture, Design of Diode bridge rectifier and filter circuit, Variable Frequency mode design, Design of main power circuit, Design of Isolator and driver circuit, Design of Protection circuit, Design of comparator.

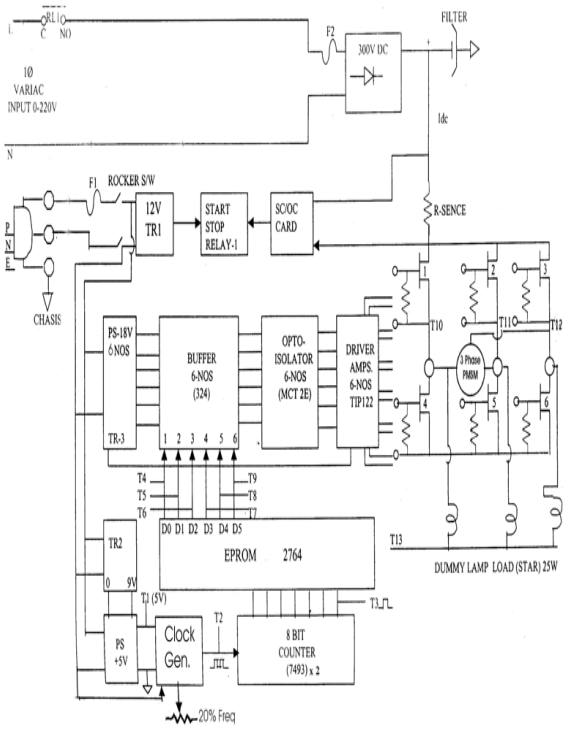

Figure 1: System Block Diagram of the PMSM Drive

A. Design of Diode bridge rectifier and filter circuit

Impute line voltage = 230 Vac
Output dc voltage = 300 vdc
Load current = 1.5 Amp.

Vm = $\sqrt{2}$ x 230
= 325.26 v

Vdc = 2 Vm/π=2 x 325.26 /π
= 207.07 (without filter)

But with Capacitor filter

V_{dc} required = 300 v

V_{dc} = V_m – (Vrpp/2)

300 = 325.26 – (Vrpp/2)

$\therefore V_{rpp}$ = 50.52 v

$V_{r\,rms}$ = Vrpp/2 $\sqrt{3}$
= 14.58 v

$\therefore$ r = V_{rms}/vdc
= 14.58/300

c = ¼ $\sqrt{3}$f. r. Rs
=¼ $\sqrt{3}$ x 50 x 0.48 x 200
= 300 µf

Selected two capacitor C_1 = 150 µf, 400 v
C_2 = 150 µf, 400 v

And are connected in parallel to get total 300 µf we have

$V_{ac\,(max)} = V_m$ = 325.26 v
$V_{o\,(min)} = V_m = V_m – V_{rpp}$
= 325.36 – 50.52
= 274.74 v

$\theta = \sin^{-1}$ V_0(min) / V_0 (max)
= $\sin^{-1}$ x 274.74 / 325.26
= 57.63^0

diode conduction angle = 90 – θ
= $90 – 57.63^0$
= 32.36^0

I_p (surge current) = T/T_1 x Idc
= $360^0 / 32.36^0$ x 1.5
= 16.68 A

3.1.1 Diodes:-

V_R (max > V_m
> 325 Volts

I_f (ave) > I_0
> 1.5 A

Isurge > I_p
> 17 A

selected diode are D_1 to D_8 = IN 5408

B. Variable Frequency mode design

In this we first consider the design of the control circuit. Let us start with the clock generator which is given to the address generator circuit. For generating the clock frequency time IC 555 is used in its astable mode.

The EPROM used in the circuit is IC 2764 from which 8 address lined are used. So one cycle of operation corresponds to 256 locations accessed by the EPROM. These address lined are generated by the counter IC 7493 to which output of 555 is connected. Thus it can be seen that the clock generator frequency is 256 times that of output frequency.

Let us assume the desired output frequency to lie in the range of 10 to 60 Hz.

Hence the timer frequency is given as

f_{min} = 10 x 256 = 2560 Hz

$f_{min} = 1 / f_{max}$ = 65104 x 10^{-5} sec.

The output voltage and the capacitor voltage waveforms are as shown in fig. 2.1

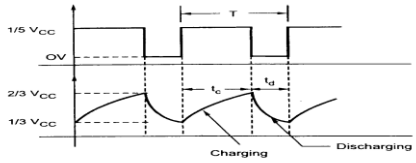

Fig. 2.1 Output voltage and capacitor voltage waveform

The capacitor is periodically charged and discharged between 2/3 V_{cc} and 1/3 V_{cc} respectively. The time during which the capacitor charges from 1/3 V_{cc} to 2/3 V_{cc} is equal to the time the output is high and is given by,

$t_c = 0.69 (R_A+R_B) C$

$t_d = 0.69 (R_B) C$

The total period for output waveform is given by,

$T = t_c + t_d = 0.69 (R_A+2R_B) C$

The frequency of oscillation is given by,

$f_0 = 1/T = 1/0.69 (R_A+2R_B) C$
$= 1.45 / (R_A+2R_B) C$

Now, consider T_{max} = 6.5104 x 10^{-5} sec.

For f_{max} = 15360 kHz.

Selecting C = 0.1 μF and R_B = 267 Ω we have

$$T_{max} = 0.69 [R_{A\,min} + 2 R_B] C$$

$$6.5104 \times 10^{-5} / 0.69 \times 0.1 \times 10^{-6} = R_{A\,min} + 2R_B$$

$$R_{A\,min} = 409.53$$

As the frequency can be varied to get variable frequency at the output, this is the minimum resistance that must be, connected in the circuit as the fixed resistance.

Selecting a resistance of 470 Ω, ¼ *w* for R_A in this position.

Now consider,

$T_{min} = 3.9062 \times 10^{-4}$ sec.

$$T_{min} = 0.69 [R_{A\,min} + 2 R_B] C$$

$$R_{A\,max} = (0.9062 \times 10^{-4} / 0.69 \times 0.1 \times 10^{-6}) - 2(267)$$

$$R_{A\,max} = 5127.15\ \Omega$$

Out of this, 470 Ω is selected as fixed resistance.

Remaining resistance = 4657.15 Ω

This remaining resistance must be variable so as to get frequency variations. Thus a pot of 4K7 is used here.

Address generator

For generating the address for the EPROM counter IC 7493 is used. It is used as a 4 bit binary counter. It is 14 pin package. In order to use their maximum count length such as decade, divide by twelve or four bit binary etc., the CKB input is connected to the Q_A output. The input count pulses are applied to CKA input and the outputs are as shown in following table. Each of these monolithic counters contain 4 master slaves flip flops and additional gating to provide a divide by two counter.

Count	Output			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

Table 1 output of 4-bit binary counter.

The 555 frequency is internally divided by two and then successively the frequency gets divided by two. The EPROM data is stored in 256 locations so address that is to be generated is also 256. with one counter 16 locations can be addressed so one more IC is connected. The Q_D output of first IC is given as clock input CKA to second IC. The corresponding outputs are tabulated as follows.

Count	Q	Q_C	Q_B	Q_A	Q_D	Q_C	Q_B	Q_A
	D	2	2	2	1	1	1	1
	2							
0	L	L	L	L	L	L	L	L
1	L	L	L	L	L	L	L	H
2	L	L	L	L	L	L	H	L
3	L	L	L	L	L	L	H	H
4	L	L	L	L	L	H	L	L
5	L	L	L	L	L	H	L	H
6	L	L	L	L	L	H	H	L
7	L	L	L	L	L	H	H	H
8	L	L	L	L	L	H	H	L
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
255	H	H	H	H	H	H	H	H

Table 2 output of 2-4 bit binary counters.

Pin 5 of each IC is provided with +5V supply. The output of these IC's act as address to the EPROM.

EPROM

The data for 120^0 mode is stored in EPROM in 256 locations. The address lines required for accessing these locations is given as

$2^N = 256$ Hence N = 8

Thus minimum 8 address lines are required. As the data is permanent and is not changing, EPROM 2764 is used for this purpose. The EPROM data generates output signals on six different data lines for the six MOSFETs. The widths of the pulses are precalculated and loaded into the EPROM. The data stored in EPROM is square pulse signal for 120^0 mode. It is taken out on D_0 to D_5 lines. For MOSFET 1 to 6, the corresponding data lines are D_0 to D_5. Thus the total data is filled in 256 locations.

There are 13 address lines out of that only 8 (A_0 –A_7) address lines are used. The rest lines are grounded. The outputs of counter Ics are connected to the respective address lines of EPROM. Total addressed generated by the EPROM are 256 which are shown in Appendix.

Out of 8 data lines, only 6 data lines 0_0- 0_5 (D_0 – D_5) are used. One cycle corresponds to 360^0

Thus we have, 360^0 = 256 location 120^0 = 83.33 ≅ 85 location

The gate pulses for the MOSFET are provided for 120^0 while for 60^0 no gate pulse is provided. The gate pulse pattern is shown in the fig.2.2.

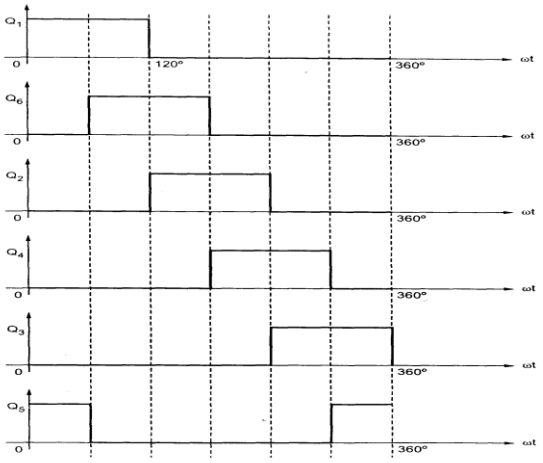

Fig. 2.2 The gate pulse pattern for the MOSFET

The data stored in EPROM in 256 locations is attached in Appendix.

C.Design of main power circuit

MOSFET bridge

While selecting MOSFET

V_{dc} > 0.707 x m_a

Vdc [let m_a = 1 (max)]

> 0.707 x 1 x 300

> 212.1 volts

V_{gs} > 12 volts

I_d > I_L max

> 2 Amps

Switching time should be as small as possible selected MOSFET is IRF 840

Snubbrer Circuit

From data sheet of MOSFET

Turn off delay = 90 ns, Fall time = 30 ns

Let to be design for maximum current capacity of MOSFET i.e. 8 Amps

C = I_0 T off / 2 V_d

= 8 x 120 ns / 2 x 212.5

= 0.0014 μF

for better performance large capacitor C to be selected. So that MOSFET voltage rises slowly and takes longer time to reach peak value of voltage capacitor C_7 to C_{14} are selected as 0.1μF, 630 volt each. The maximum load current is taken to be 8 A and maximum voltage reading of MOSFET is 600 volt,

Free wheeling Diode

I_f (ave) = 8 A

V_K = 600 V

Selected diodes D_{17} to D_{24} = IN5408

Series resister with capacitor should be chosen so that the peak current through it is less than reverse recovery current. I_n of the free wheeling diodes

V_d / R_s = I_n

But generally

I_n is limited 0.4 I_0

R = V_d /0.4 I_0 = 500 / 0.4 x 8

= 156.75 Ω

Selected resister R_7 to R_{14} = 150Ω 2 w each.

D.Design of Isolator and driver circuit

The gate pulse is applied to isolator through buffer. The used buffer using I_C LM324, which has following features

1) Eliminates need for dual power supply.
2) Compatible with all forms of logic.
3) Internally frequency compensated for unity gain.
4) Low input bias current = 45 nA
5) Low input offset voltage = 2 mv dc
6) Differential input voltage = ±Vcc
7) Large output voltage swing = 0 to (+V – 1.5) V

Specifications:

Output current = 40 mA dc

Supply voltage = 32 v or ± 16 v dc

Selected opto Coupler is MCT2E which has got IRED and phototransistor internally. The maximum forward current for LED = 20 mA

Peak output voltage of LM324 will be = 12 – 1.5 = 10.5

$V_i \cong 11$ v

Let maximum current for LED to be selected as 8 mA

R = V_i – V_f (LED) / I_f

= 11 – 1.8 (max) / 8 mA

= 1150 Ω

selected R = 1.1 kΩ ¼ w

with this value

I_f (max) = 11 – 1.6 (typ) / 1.1 kΩ

= 8.54 mA

which is acceptable value for MCT2E

selected R_{20} to R_{23} & R_{44} to R_{47} = 1.1 kΩ ¼ w each.

MCT2E requires supply voltage = 15 Vdc

So we design power supply for the rating 100 mA.

Using transformer of 12-0 secondary voltage.

V_m (sec) = √2 x 12 = 17 V

Selected ripple voltage V_{rpp} = 0.5 V

V_{dc} = V_m – 0.7 (diode drop) – (0.5 /2)

= 16 V

r = V_{rms} / Vdc

= V_{rpp} / 2 √3 Vdc

= 0.5 / 2√3 x 16

= 0.009

c = 1/ 4√3 x f x r x R_L

= 1 / 4√3 x 50 x 0.009 x (16/0.1)

= 2000 μF

selected value of c = 2200 μF / 25 V

with this value

c = 1/ 4√3 x 2200 μF x 160

= 0.0082

V_{rms} = r x Vdc

= 0.0082 x 16

= 0.1312 V

V_{rpp} = 0.45 V

Selected capacitor C_{12} to C_{20} and C_{21} to C_{23} = 2200 μF / 25 V

Diodes

PIV > Vm
> 17 V
I_f > I_1
> 100 mA

selected diodes D_{26} to D_{57} are IN4007

Transformer

Transformer used here is a signal core six isolated secondary with rating 12-0, 500 mA each.

E. Design of Protection current

This circuit needs +12 V dc power supply for its operation. We can use IC7812 regulator IC for this purpose.

Here V_{out} = 12 V
ΔV = 2 V
V_{in} = V_{out} + ΔV
= 12 + 2 = 14 V

i.e., unregulated dc input voltage is 14 V

Assuming ripple voltage is 14 V

V_{dc} = 14 + V_{rpp} / 2
= 14 + 5/2 = 16.5 V

V_m (rectifier) = 14 + 5 = 19 V

V_m (secondary) = 19 +2 V_d = 19 + (20 x 0.7)
= 19 + 1.4 = 20.4 V

Assuming transformer regulation to be 10%

V_m (secondary) = 20.4 (10% of V_m (secondary))
= 20.4 + 2.04
= 22.44 volts

$V_{m\,ac}$ = 230 V_{rms}

V_m (primary) = 230 x $\sqrt{2}$ = 325 V

Turns ratio = V_m (primary) / V_m (secondary)
= 325 / 22.44
= 15:1

Now,

V_{rms} = V_{rpp} / $2\sqrt{3}$ = 5/$2\sqrt{3}$ = 1.443 V

Ripple factor r = V_{rms} / V_{dc} = 1.443 / 16.5
= 0.0875

Assuming I_{dc} = 500 mA

Let us calculate the value of filter capacitor.

C_3 = C_1 = I_{dc} / $4\sqrt{3}$ .f. V_{rms}
= 500 x 10^{-3} / 4 x $\sqrt{3}$ x 50 x 1.443
= 999.7 µF.

selecting value of C_3 = 1000 µF / 25 V

Actually V_{dc} = 4 x f x CR_1 / (1 + 4 x f x C x R1) x V_m
= 0.868 V_m
V_{dc} = 0.868 x 22.44
= 19.48 V

Selection of Diodes

I peak = [2.63 $\sqrt{r}$ / (1 + $\sqrt{3}$ r)] V_m C ω
= [2.63 x 0.0875 / (1 + $\sqrt{3}$ x 0.0875)] x
22.44 x 1000 x 10^{-6} x 2π x 50
= 4.63 A

I (avg) = I_l / 2 = 500 / 2 = 250 mA

PIV = V_m = 22.44 V

IN4007 diodes are selected which have
I(avg) = 1 A & I peak = 10A

Same diodes is used across relay coil as a free wheeling diode.

Overload and short circuit current is assumed to be 3 A

Selected Rsense = 1 Ω

Power rating R sense = I^2R = 3^2 x 1
= 9 W

R sense is selected as 1Ω, 10 W

After R sense diode bridge is kept so as to obtained pure dc voltage. Again IN4007 diodes are used in bridge. After that RC combination with value

R_{68} = 10 kΩ & C_{25} =10µF / 25 V is used as dummy load.

Design of comparator

Select R_{70} to R_{71} = 1kΩ

To adjust the voltage at point x , so that it will be equal to voltage at output across R_{69}. one preset is used. Its value is 4k7. Transistor SL100 is used to drive the relay. One pull up resistor of 1k value is used as the output of comparator.

III . Experimental Results

Table No.1:Variation in the speed of the motor as a function of inverter frequency

Sr. No.	Time (m.s.)	Frequency (Hz)	Expected Speed (rpm)	Measured Speed (rpm)	Voltage (Volts)
1	30	33.3	999	1010	265
2	25	40	1200	1226	270
3	22	45.4	1362	1380	270
4	20	50	1500	1520	270
5	18	55.5	1665	1682	270
6	17	59	1770	1790	270

Table No.2: Variation in the speed of the motor as a function of load at constant frequency of 33.3 Hz

Sr. No.	Load (gm)	Expected Speed (rpm)	Measured Speed (rpm)	Voltage (volts)
1	500	999	1010	270
2	1000	999	1010	270
3	1500	999	1010	270
4	2000	999	1010	270
5	2500	999	1010	270
6	3000	999	1010	270

Table No.3: Variation in the speed of the motor as a function of load at constant frequency of 50 Hz.

Sr. No.	Load (gm)	Expected Speed (rpm)	Measured Speed (rpm)	Voltage (Volt)
1	500	1500	1520	270
2	1000	1500	1520	270
3	1500	1500	1520	270
4	2000	1500	1520	270
5	2500	1500	1520	270
6	3000	1500	1520	270

TABLE I

Sr. No.	Load (gm)	Frequency (Hz)	Speed (rpm)	Torque (N-m)	Output Power (W)
1	500	33.3	1010	0.14715	15.55
2	1000	33.3	1010	0.2943	31.12
3	1500	33.3	1010	0.4414	46.68
4	2000	33.3	1010	0.5886	62.19
5	2500	33.3	1010	0.7357	77.81
6	3000	33.3	1010	0.8829	93.38

TABLE II

Sr. No.	Load (gm)	Frequency (Hz)	Speed (rpm)	Torque (N-m)	Output Power (W)
1	500	50	1520	0.14715	23.47
2	1000	50	1520	0.2943	46.84
3	1500	50	1520	0.4414	70.25
4	2000	50	1520	0.5886	93.68
5	2500	50	1520	0.7357	117.1
6	3000	50	1520	0.8829	140.5

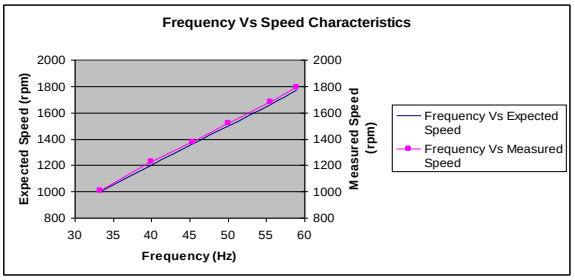

Fig3.1 Frequency Vs Speed characteristics

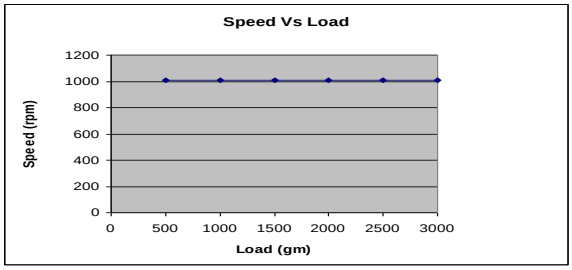

Fig. 3.2 Speed Vs Load Characteristics at Constant Frequency = 33.3 Hz

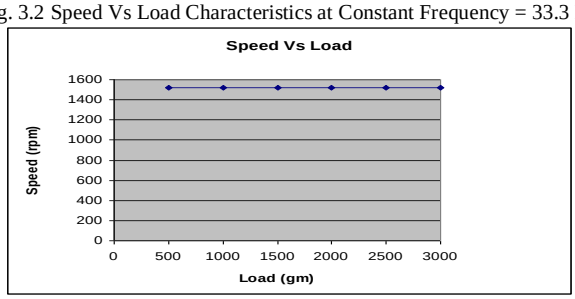

Fig. 3.3 Speed Vs Load Characteristics at Constant Frequency = 50 Hz

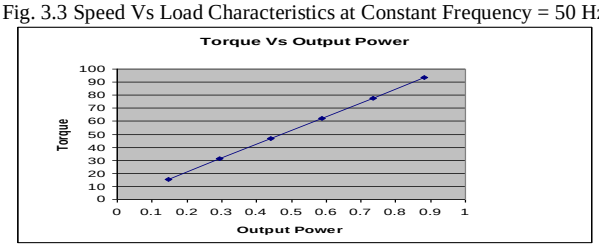

Fig. 3.4 Torque Vs Output Power at frequency 33.3 Hz

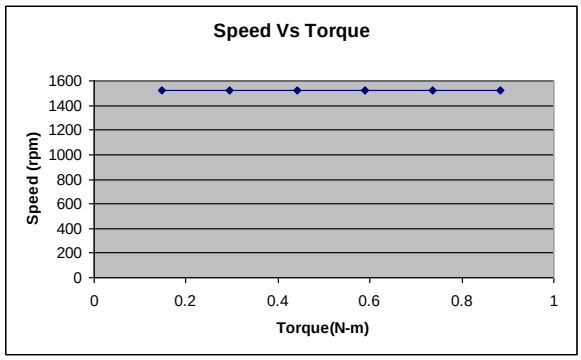

Fig. 3.5 Speed Vs Torque at Constant Frequency = 50 Hz

IV . Conclusion

A Design of PMSM drive system for EPS application has been presented in this paper . we conclude that, by varying the inverter frequency, the speed & Torque of the motor also gets varied. If the frequency is kept constant at particular value, the speed of the motor also remains constant, irrespective of the load. It runs at synchronous speed. But torque varying irrespective of the load. The experimental results prove that the PMSM drive presented in this paper is suitable for Electric Power Steering used in Automotive Application.

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